6.012 Electronic Devices and Circuits

Answers for Exam No. 2 - Spring 2000
(Ave = 72, □ = 13, n = 123)

Problem 1:

a) p-type, because $V_T > V_{FB}$.

b) Accumulated, because $0 < V_{FB}$.

c) The surface is depleted for v_{GB} between V_{FB} and V_T, so the range is $1\ V < v_{GB} < 3\ V$.

d) n-channel, because we know that in general $\mu_e > \mu_h$, and K varies as μ/L, and thus the device with the greater μ will have the larger L.

e) The ratio of the lengths matches the ratio of the mobilities, so the ratio is 2.

f) i) n-channel because the device with the longer gate has the larger gate area and therefore the larger C_{gs}. According to Part d this is the n-channel device.

ii) They are similar, because C_{gd} depends on the parasitic fringing capacitance at the drain end of the gate and this scales as W, which is the same in both.

g) i) p-channel, because channel length modulation will be more important in the devcie with the shorter gate lenth, and thus the shorter device will have the greater slope in its output characteristics.

ii) Transistor B, because a large Early effect, by which we mean a large slope in the output characteristics, will have a smaller Early voltage, V_A.

h) p-channel, because K depends on the product of μ and W, and thus the device with the lower μ will have the greater W.

i) They are similar because $g_m = (2K|I_D|)^{1/2}$, and we are told that K and $|I_D|$ are the same in both devices.

j) They are similar, because the gate (channel) lengths are the same and thus the impact of channel length modulation will be the same.

Problem 2:

a) i) In accumulation we measure $□_{ox}A/t_{ox}$, which we find here to be approximately 1.1×10^{-11} F (11 pF).

ii) Smaller, because now the "new" charge in the Si is added farther away for the gate metal, making the equivalent capacitor wider, and its value smaller.

b) i) Inverted, because the device is n-channel and the voltage is above the threshold voltage of 1 V.

ii) Electrons, since the device is n-channel.

iii) The mobile charge is $-A(□_{ox}/t_{ox})(v_C - V_T)$, which we compute to be -2.2×10^{-11} coul.

iv) Greater than, because the gate charge equals the channel charge plus the inversion layer charge.

c) i) We must have at least the desired V_C on A, so $V_A \geq 3$ V, and the voltage on the gate, i.e. V_B, must be at least V_T higher that the voltage we wish to reach. Thus we must have $V_B \geq 4$ V.

ii) If the capacitance is a constant C_L, then we have that $dv_C(t)/dt = i_D/C_L$. The issue is finding which expression to use for i_D, the linear region or saturation region value (or one part of the time and the other the rest). To answer this we check if we are in saturation, $v_{DS} \geq v_{GS} - V_T$. Noting that v_{DS} is $v_A - v_C$, and v_{GS} is

v_B - v_C, and putting these expressions into our inequality, we find that it becomes $v_A \geq v_B - V_T$, which is always true since $v_A = v_B = 5$ V, and $V_T = 1$ V, and thus the MOSFET is always in saturation. Thus, $i_D = K(v_{GS} - V_T)^2/2 = K(v_B - v_C - V_T)^2/2$, and the equation is: $dv_C(t)/dt = K(v_B - v_C - V_T)^2/2C_L$.

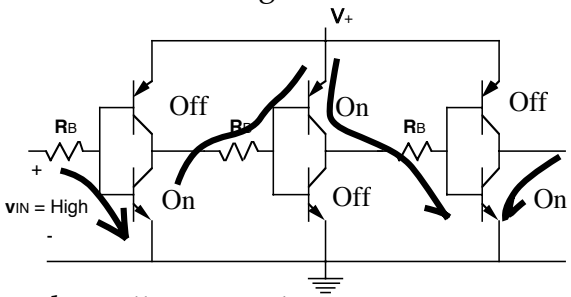
Problem 3:

a) i) pnp: Cutoff, because $v_{EB}(pnp) = 0$
npn: Saturated, because $v_{BE}(npn)$ is large and $i_B(npn) > i_C(npn)$
Low, with a value of $\approx V_{CE,SAT}$, or ≈ 0.2 V.

ii) pnp: Saturated, because now $v_{EB}(pnp)$ is large and $|i_B(pnp)| > |i_C(pnp)|$
npn: Cutoff, because $v_{BE}(npn) = 0$.
High, with a value of $\approx 1 - |V_{CE,SAT}| \approx 0.8$ V.

iii) Yes, because the output is high when the input is low, and low when the input is high.

b) See the arrows on the figure below:



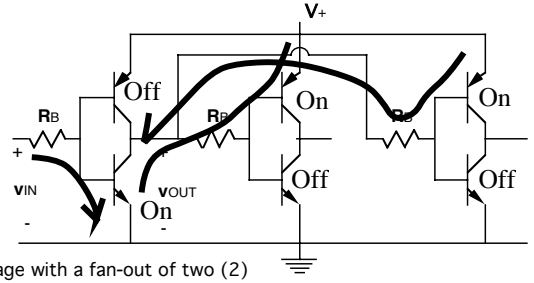
c) i) At the collector node: $I_C = I_B = \beta_F I_F - I_R$; at the emitter node: $I_E = -2I_B = \beta_R I_R - i_F$. Solving for I_B: $I_B = [(1 - \beta_F\beta_R)/(2 - \beta_R)]\, I_F \approx [(1 - \beta_F\beta_R)/(2 - \beta_R)]\, I_{ES} \exp(qV_{BE}/kT) \approx 10^{10}\, I_{ES} = 1.73 \times 10^{-5}$ A (4.57×10^{-5} A if you do not use the 60 mV approx.).

$V_{BC} \approx (kT/q) \ln (I_R/I_{CS})$ and solving our two node equations for I_R in terms of I_F we have $I_R = [(2\beta_F - 1)/(2 - \beta_R)]I_F \approx [(2\beta_F - 1)/(2 - \beta_R)]\, I_{ES} \exp(qV_{BE}/kT)$. Using this we have $V_{BC} \approx V_{BE} + (kT/q) \ln [(2\beta_F - 1)/(2 - \beta_R)] \approx 0.592$ V.

Finally, $V_{CE} = V_{BE} - V_{BC} = 0.008$V.

ii) This is a way of calculating the low logic level more accurately. One would need to know RB to do a full determination of this and of the high level.

d) Higher, because with more collector current, i_C, the BJT will not be as far into saturation and v_{CE} will be larger. To see this it is useful to add the arrows to the figure (below) and note that the collector current of the saturated transistor is now larger:



Stage with a fan-out of two (2)

e) There is no loading of one stage by another because the input resistance of a CMOS inverter is infinite and thus it does not draw current from (or supply current to) the preceeding stage.